detection means recited in claims 14, 17 and 20 are indeed illustrated in the original drawings and the replacement formal drawings filed on March 16, 2005.

The specification describes the present invention in the form of various Examples. The Applicants first direct the Examiner's attention to the "Phase polarity change point detection circuit 3" illustrated in Figure 1 and its accompanying description in lines 23-30 on page 9 of the substitute specification. Lines 23-20 on page 9 of the substitute specification provide:

> The phase polarity change point detection circuit 3 has the functions of determining the polarity of the change in phase (whether this change is positive or negative) which is detected by the phase change detection circuit 2, detecting the point in time (timing) when this polarity changes, and providing the results of this detection as output to the change point statistical processing circuit 4. Note that such a polarity change point may be acquired by detecting the timing at which the polarity of the phase change which is detected by the phase change detection circuit 2 inverts (changes from positive to negative, or changes from negative to positive), and namely, this timing can be used as the polarity change point. (emphasis added)

Accordingly, the positive/negative change timing detection means as recited in the claims is clearly illustrated by the phase polarity change point detection circuit 3 in Figure 1.

The Applicants also direct the Examiner's attention to the "change point extraction circuit T5" illustrated in Figure 4 and its accompanying description in lines 3-20 on page 17 and lines 19-23 on page 20 of the substitute specification. In particular, lines 19-23 on page 20 of the substitute specification provide:

> [I]n this Example, the change point extraction circuit T5 shown in FIG. 4 above has the function of detecting the timing at which the change in phase of the preamble pattern that is contained in the received burst signal changes between positive and negative, and constitutes the "positive/negative change timing detection means" which is referred to in the present invention. (emphasis added)

Accordingly, the positive/negative change timing detection means as recited in the claims is clearly illustrated by the change point extraction circuit T5 in Figure 4.

The Applicants also direct the Examiner's attention to the "synchronization establishment circuit 58" illustrated in Figure 13 and the description in lines 22-27 on

page 22 of the substitute specification. Lines 22-27 on page 22 of the substitute specification provide:

> [T]he "positive/negative change timing detection means" and "synchronization establishment means" which are referred to in the present invention are constituted in this Example by the functions of the synchronization establishment circuit 58 detecting the timing at which the positive/negative polarity of the phase changes in the preamble pattern that is contained in the received burst signal, and establishing clock synchronization from this received burst signal based on the detected timing. (emphasis added)

Accordingly, the positive/negative change timing detection means as recited in the claims is clearly illustrated by the synchronization establishment circuit 58 in Figure 13.

Furthermore, the Applicants also direct the Examiner's attention to the "demodulator 73" in Figure 15 and the description in lines 20-27 on page 25 of the substitute specification. Lines 20-27 on page 25 of the substitute specification provide:

> [I]n the base station 61 of this Example, the function whereby the demodulator 73 detects the timing of the positive/negative polarity change in the change in phase of the preamble pattern that is contained in the received burst signal, and establishes clock synchronization from the received burst signal based on the detected timing, and the function whereby the (unique word and data contained in the) received burst signal is demodulated according to the established synchronization timing constitute the "positive/negative change timing detection means," the "synchronization establishment means" and the "demodulation means" which are referred to in the present invention. (emphasis added)

Accordingly, the positive/negative change timing detection means as recited in the claims is clearly illustrated by the demodulator 73 in Figure 15.

In view of the above, the Applicants respectfully submit that the positive/negative change timing detection means as recited in the claims is clearly illustrated in Figures 1, 4, 13 and 15.

Therefore, the Applicants respectfully request the Examiner to withdraw the objection to the drawings.

Accordingly, in view of the Examiner's assertion that claims 14-22 are allowed and having respectfully traversed the objections to the drawings, the Applicants

respectfully submit that the present application is now clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Response, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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